AMENDMENTS TO THE CLAIMS

Please amend the claims as follows.

1.   (Currently Amended) A method for reducing signed load latency in transfer of data from a cache memory to another element in a microprocessor comprising:

   transferring data from ~~a~~ the cache memory to an aligner;

   generating a sign bit for the data; and

   transferring the sign bit to the aligner via a bypass,

      wherein transferring data and transferring the sign bit occur in parallel.

2.   (Previously Presented) The method of claim 1, further comprising:

   adjusting the data during transfer to the aligner via a data path; and

   selecting the sign bit during transfer to the aligner via the bypass.

3.   (Original) The method of claim 2, further comprising:

   selectively processing a part of the data for use in generating the sign bit.

4.   (Previously Presented) The method of claim 3, further comprising:

   processing the part of the data selected for use in generating the sign bit based on an instruction from a CPU.

5.   (Currently Amended) An apparatus for reducing signed load latency in transfer of data from a cache memory to another element in a microprocessor, comprising:

   a data path connecting the cache memory to an aligner; and

   a bypass connecting the cache memory to the aligner;

wherein data is transferred from the cache memory to the aligner via the

data path and a sign bit for the data is transferred from the cache

memory to the aligner via the bypass, and

wherein the transfer of data via the data path and the transfer of the sign

bit via the bypass occur in parallel.

6.   (Previously Presented) The apparatus of claim 5, further comprising:

a select component for providing signals to choose the sign bit for the data.

7.   (Original) The apparatus of claim 5, wherein the bypass comprises:

a sign multiplexer; and

a real-sign multiplexer.

8.   (Original) The apparatus of claim 6, wherein the select component provides a signal to

choose a part of the data and to generate the sign bit for the data based on an instruction

from a CPU.

9.   (Original) The apparatus of claim 5, wherein the aligner comprises a plurality of sub-

aligners.

10.   (Currently Amended) An apparatus comprising:

means for transferring data from a cache memory to an aligner;

means for generating a sign bit for the data;

means for transferring the sign bit to the aligner via a bypass;

means for adjusting the data during transfer to the aligner via a data path;

means for adjusting the sign bit during transfer to the aligner via the bypass;

means for selectively processing a part of data for use in generating the sign bit;
and

means for selectively processing the part of the data selected for use in generating

the sign bit based on an instruction from a CPU,

wherein the transfer of data via the data path and the transfer of the sign bit via

the bypass occur in parallel.

11.   (Currently Amended) An apparatus comprising:

a data path connecting a cache memory to an aligner;

a bypass connecting the cache memory to the aligner;

wherein data is transferred from the cache memory to the aligner along the

data path and a sign bit for the data is transferred from the cache

memory to the aligner along the bypass, and

wherein the transfer of data via the data path and the transfer of the sign

bitvia the bypass occur in parallel;

a select component for providing signals to choose the sign bit for the data,

wherein the select component comprises:

a sign multiplexer; and

a real-sign multiplexer, and

wherein the select component provides a signal for choosing a part of the

data to generate the sign bit for the data based on an instruction

from a CPU; and

wherein the aligner comprises a plurality of sub-aligners.